Remarks & Arguments

In the Office Action, the Examiner noted that Claims 1-8 and 10-37 are pending in the application, and that Claims 1-8 and 10-37 are rejected. By this amendment, Claims 1, 2, 6, 8-11, 19, 22, 23, 30 and 31 have been amended. The amendments to the claims do not add new matter to the application. The Examiner's rejections are traversed below.

Rejections Under 35 U.S.C. 112, Second Paragraph

Claims 1, 11, 22 and 30 stand rejected under 35 U.S. C. 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office alleges that the limitation of "a description of hardware resources" (claims 1 & 30), "a test based description" (claims 11 & 22), "configuration information" (claims 1, 11, 22 & 30), "a selected configuration" (claims 1, 11, 22 & 30) and "interrupt vector" (claim 30) are indefinite.

First, the Applicants respectfully assert that the Office's rejection is a bare allegation with no showing of how the claimed limitation may be interpreted in "many ways." The MPEP states, with regard to this contention, that "an analysis as to why the phrase(s) used in the claims is "vague and indefinite" should be included in the Office action" (MPEP 2173.03). The statement that it "would cause a claim construction problem because one can interpret the claimed limitations in many ways" is not an analysis as to why the phrases used in the claims are vague and indefinite. Instead it is a statement of the problem cause if the language is indefinite.

A proper analysis would show how the language can in fact be interpreted in ways inconsistent with the Applicant's disclosure. Furthermore, the Office needs to provide an analysis for each limitation as to why each particular limitation is indefinite. Accordingly, the Office has failed to make a prima facie case.

Second, the MPEP states that "the invention set forth in the claims must be presumed, in the absence of evidence to the contrary to be that which applicants regard as their invention" (MPEP 2172). Since, the Office has failed to make any showing of evidence to the contrary it "must be presumed" that the invention set forth in the claims is what Applicants regard as their invention. The MPEP also states that "a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought" (MPEP 2173.01). The rejection of the limitations of "a description of hardware resources", "a test based description", "configuration information", "a selected configuration" and "interrupt vector," without any showing as to how the limitations are indefinite, is clearly an improper rejection based "solely because of the type of language used."

The Applicants also not that the MPEP states that the "Examiners are encouraged to suggest claim language to applicants to improve the clarity or precision of the language used." In particular, "if the language used by applicant satisfies the statutory requirement of 35 U.S.C. 112, second paragraph, but the examiner merely wants the applicant to improve the clarity or precision of the language used, the claims must not be rejected under 35 U.S.C. 112, second paragraph, rather, the examiner should suggest improved language to the applicant" (MPEP

2173.02). However, the Office has made no attempt to suggest language that is more "clear and concise."

The MPEP also states that the test for definiteness under 35 U.S.C. 112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification" (MPEP 2173.02). The term "a description of hardware resources" of said microcontroller is described in the specification at page 11, line 7 through page 13, line 2. The term "a text based description" of dynamically configurable blocks is described in the specification at page 12, line 17 through page 13, line 2. The term "configuration information" is described in the specification at page 13, line 14 through page 14, line 8. The term "a selected configuration" is described in the specification at page 13, lines 4-12. The term "interrupt vector" is described in the specification at page 14, lines 1-8. Based upon the disclosure in the specification regarding the rejected limitations, Applicants respectfully contend that those skilled in the art understand what is claimed. The Office has failed to advance any argument as to why the disclosure related to the rejected limitations does not provide those skilled in the art with the necessary understanding.

The MPEP also states that "the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor's contribution to the art" (MPEP 2173.02). When the rejected limitations and their interactions with other limitations in the claim are considered the claimed subject matter is particularly clear and concise to those skilled in the art. For example, those skilled in the art understand that the "description of hardware resources" are descriptive representations in words of various available configurations

of hardware resources of the microcontroller. As amended, "a description of hardware resources" has been further limited to "text readable." "A description of hardware resources" has also been further limited in Claim 30 to exclude "microcontroller executable" descriptions of hardware sources. Similarly the other rejected limitations are clear and concise when the totality of all the limitations of the claims and their interaction with each other are considered.

The Office also states that "all dependent claims on the based claims that are not described are also virtually rejected based on the rejected based claims. Applicants have done an electronic search of Title 35 of the United States Code, Title 37 of the Code of Federal Regulations, the MPEP and www.uspto.gov for the term "virtual rejection," "virtually rejecting" and "virtually rejected." The Applicants cannot find any legal basis for "virtually rejecting" any claims. The Applicants therefore request that the Office provide the legal basis for making a "virtual rejection." In the absence of any such legal authority, Applicants respectfully assert that the indefinite rejection with regard to "all dependent claims" is invalid. Furthermore, the Applicants note that a number of the dependent claims further limit the alleged indefinite limitations. Therefore, the Office is required to make a separate prima facie case of indefinite for each dependent claim that further limits one of the alleged indefinite terms. Thus, even if there is such a thing as a "virtual rejection," the Office cannot properly apply it to "all dependent claims."

The Applicants also note for the record that the alleged indefinite limitations were present in the claims as originally filed. The Examiner is now raising the indefinite rejection in the fifth office action. The Regulations state that "the examiner's action will be complete as to all

matters" (37 CFR 1.104; See also MPEP 707.07(g)). Accordingly, the Applicants object to the Primary Examiners piecemeal examination of the present application.

Rejections Under 35 U.S.C. 102

Claims 11, 13-17 and 19-29 stand rejected under 35 U.S.C. 102 as being anticipated by U.S. Patent No. 6,460,172 to Farre. Applicants respectfully traverse the rejection of Claims 1, 13-17 and 19-29 on the basis that the relied upon reference does not teach every element in the independent Claims.

Claims 11, as amended, recites a method for configuring a microcontroller that includes "accessing **a text based description** of said dynamically configurable blocks" wherein "said text based description is **not executable software**." The Office refers to Figure 1 and its description in Farre to support the assertion that Farre teaches a system that includes "a processor, memories, configurable blocks including digital blocks, analog blocks that are selectable from a set of **library macros** and cells to configure and dynamically reconfigure whole or partial systems." More particularly, the Applicants respectfully point to Farre at col. 3, lines 31-38 in which Farre discloses that "the invention ... comprises ... a suitable set of CAD tools to easily program it, and a set of library macros and cells which support a number of typical applications to be easily mapped into the FPD and migrated to an ASIC." Those skilled in the art appreciate that a macro is executable software.

Furthermore, Farre, at col. 2, lines 33-39, discloses "an integrated emulator that links **the user circuit entered with schematics and/or a Hardware Description Language (HDL)** with

a hardware/software co-emulation and open simulation engines, in a way that makes [it] possible to specify and co-emulate hardware and mixed-signal (analog and digital) general purpose applications in real time over the single silicon chip. At col. 2, lines 40-46, Farre discloses "a new approach to system prototyping of mixed signal applications, comprising a mixed signal device with on-chip microprocessor, **suitable user-friendly CAD tools to program it and a set of library macros** and applications to provide an easy path for migration." At col. 2, lines 59-67 Farre discloses "The CAD design flow includes mixed signal design specification, simulation, automatic technology mapping, device programming, and real time emulation (probing of internal signals), so **the user can work at system level with microprocessor code** and mixed signal hardware using an integrated design tool. Finally **library macros** are provided to support typical user applications to provide an immediate way to migrate the application to ASIC after prototyping." At col. 3, lines 62-67, Farre discloses "a large set of **library macros** provides optimized solutions to typical design needs, ..., **from HDL to even manual placement and routing**. A parallel ASIC library is also supported to make the migration to ASIC much easier than in normal prototyping." Furthermore, Farre claims "**the first CAD tools include schematic capture**, technology mapping, placement, routing and device programming" and "**the second CAD tools including schematic capture**, technology mapping, placement routing, and device programming." Accordingly, Farre only discloses accessing "microprocessor code." "macros." "schematics." And/or "HDL" which are non-text based descriptions and/or executable software.

For all the reasons advanced above, Applicants respectfully assert that Farre does not disclose a "text based description" that is not "executable software." Applicants therefore submit

that Claim 11 is patentable over Farre. Accordingly, Applicants request that the anticipation rejection of Claim 11 be withdrawn and that Claim 11 be allowed.

Claims 13-17 and 19-21 are allowable by virtue of their dependency on respective base Claim 11, as well as the additional elements they recite. Accordingly, Applicants respectfully request that the anticipation rejection of Claims 13-17 and 19-21 be withdrawn and that Claims 13-17 and 19-21 be allowed.

Claims 22, as amended, recites a system for implementing a method for configuring a microcontroller that includes "accessing **a text readable description** of a plurality of dynamically configurable blocks." As discussed above with respect to Claim 11, Farre only discloses accessing "microprocessor code" "macros" "schematics" "HDL" and/or "manual placements" which are non-text based descriptions and/or executable software. Accordingly, Farre does not disclose a "text readable description." Applicants therefore submit that Claim 22 is patentable over Farre and request that the anticipation rejection of Claim 22 be withdrawn and that Claim 22 be allowed.

Claim 23 is allowable by virtue of its dependency on respective base Claim 22, as well as the additional elements it recites. In particular, Farre does not disclose that the "text readable description" includes "a non-executable software data structure." Instead, Farre discloses "a set of library macros" which are executable software. Accordingly, Applicants respectfully request that the anticipation rejection of Claim 23 be withdrawn and that Claim 23 be allowed.

Claims 24-29 are allowable by virtue of their dependency on respective base Claim 22, as well as the additional elements they recite. Accordingly, Applicants respectfully request that the anticipation rejection of Claims 24-29 be withdrawn and that Claims 24-29 be allowed.

Rejections Under 35 U.S.C. 103

Claims 12 stands rejected under 35 U.S.C. 103 as being obvious in view of the combination of U.S. Patent No. 6,460,172 to Farre and U.S. Patent No. 6,578,174 to Zizzo. Applicants respectfully traverse the rejection of Claim 12 on the basis that the relied upon references do not teach every element and in addition that there is no suggestion or motivation to combine the references.

The Office acknowledges that Farre does not teach or suggest that the description of the dynamically configurable blocks are compliant with the extensible markup language (XML). However, the Office refers to Zizzo at col. 7, 9 to support the assertion that Zizzo teaches "a method and system for chip design using remotely located resources comprising circuit design platform to facilitate the design of an IC by making it easier for designers to locate and incorporate available virtual component blocks into new designs including using a universal data interface format or mark-up language (XML) is preferably used as a primary data interface between the various component of the system and the details XML are well-known to those in the art of computer programming." The applicants respectfully disagree with the Office's position, and suggest that the relied upon passages do not support the Office's assertion. In particular Zizzo only discloses that XML is used to communicate information between remotely

located resources. The resources are distributed workstation and servers of the circuit design platform used to design the IC and not the "dynamically configurable blocks" of the IC being designed. Accordingly, if there was a motivation or suggestion to combine the teaching of Farre and Zizzo, the references would instead teach that "a set of library macros" (e.g., a set of executable programs) are communicated between the user workstation and one or more servers 260, 232, 234, 236, 240, 244 using XML as part of the communication protocol (e.g., secure XML tunnels (col., lines 30-33)).

Furthermore, Applicants assert that Farre only discloses accessing "microprocessor code" "macros" "schematics" "HDL" and/or "manual placements" which are non-text based descriptions and/or executable software. There is no suggestion or motivation in Farre or Zizzo of how to replace the "schematic capture" using "microprocessor code" "macros", "HDL" or "manual placements" with the alleged XML description of Zizzo.

For each of the reasons set forth above, Applicants respectfully submit that Claim 12 is patentable over Farre in view of Zizzo. Accordingly, Applicants request that the obviousness rejection of Claim 12 be withdrawn and that Claim 12 be allowed.

Conclusion

For all the reasons advanced above, Applicants respectfully submit that the present application is in condition for allowance and that action is earnestly solicited. The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

The Commissioner is hereby authorized to charge any additional fees, which may be required for this amendment, or credit any overpayment, to Deposit Account 23-0085. In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account 23-0085.

Respectfully submitted,

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